

Specification for Display Module

31.5 inch E Ink Spectra 6 Display Module

Model No.: ND315EPN25601440-A01

Product Specification V03

2560 x 1440 pixels | Six colors | Reflective display

Customer Approval

Customer	
Approval By	
Date of Approval	

Model Number Structure

Example: ND070TSC1024600-A01

ND	070	TS	C	1024600	A	01
Brand	Size	Family	Structure	Resolution	Variant	Revision

Code Structure

Code	Meaning	Example / Description
ND	Brand	NoseDisplay
070	Size	7.0-inch nominal diagonal size
TS	Family	Product family code
C	Structure	Capacitive touch (CTP/PCAP)
1024600	Resolution	1024 x 600 pixels
A	Variant	Different base product variant
01	Revision	Compatible update of the same variant

Product Family Codes

Code	Family	Code	Family
EP	ePaper Displays	HM	Industrial HMI
ES	ESP32 Displays	HP	HDMI & Pi Displays
TS	Small / Medium TFT	TL	Large Size TFT LCD Module
TB	Bar-Type TFT	TF	Transflective TFT
TR	Round TFT	AM	AMOLED Displays
MC	Character LCD	MG	Graphic LCD
MS	Segment LCD	MP	PMOLED Displays

Structure Codes

Code	Structure	Code	Structure
N	No Touch	G	Cover Glass / Lens
R	Resistive Touch (RTP)	C	Capacitive Touch (CTP/PCAP)
H	Housed / Enclosed	K	Rotary / Knob
D	Development Kit		

Variant / Revision: A/B/C = variants; 01/02/03 = compatible revisions.

Size: SSS = nominal diagonal size group.

Family: Integrated products use the main platform family (e.g., ES / HP).

Structure priority: N -> G -> R/C -> H -> K -> D (low -> high); use the highest applicable code.

Exceptions: MC/MS may use format codes; EOL keeps the original manufacturer model.

1. General Description

ND315EPN25601440-A01 uses the ND320ENM-A01, a 31.5-inch reflective electrophoretic display module using E Ink Spectra 6 technology and an active-matrix TFT substrate. It provides a 2560 x 1440 pixel array in landscape format. Red, green, blue, yellow, black and white image states are produced with the matching controller and waveform. The display is bistable and uses ambient light for viewing.

No.	Feature	Details	Unit
1	Display size	31.5 diagonal	inch
2	Display technology	E Ink Spectra 6 / reflective	-
3	Resolution / aspect ratio	2560 (H) x 1440 (V) / 16:9	pixels
4	Display colors	Red / green / blue / yellow / black / white	-
5	Active area	696.32 (H) x 391.68 (V)	mm
6	Pixel pitch / density	0.272 x 0.272 / 94 ppi	mm
7	Outline dimensions	703.52 (H) x 406.48 (V) x 0.85 (D)*	mm
8	Module weight	582 ± 20	g
9	Surface treatment	Anti-glare protective sheet	-
10	Operating temperature	0 to +50	°C
11	Storage temperature	-25 to +60	°C

* Thickness excludes masking film; local PCB and component heights are shown in the mechanical drawing. Outline dimensions are not the full component envelope.

Mechanical dimensions for ND320ENM-A01 are listed below in millimeters. Refer to Section 3 for the drawing; do not scale the illustration.

No.	Mechanical item	Nominal	Tolerance	Unit
1	Outline width	703.52	±0.30	mm
2	Outline height	406.48	±0.30	mm
3	Active area width	696.32	±0.10	mm
4	Active area height	391.68	±0.10	mm
5	Thickness without film	0.85	±0.09	mm
6	Thickness with film	0.91	±0.09	mm
7	General tolerance*	-	±0.3	mm

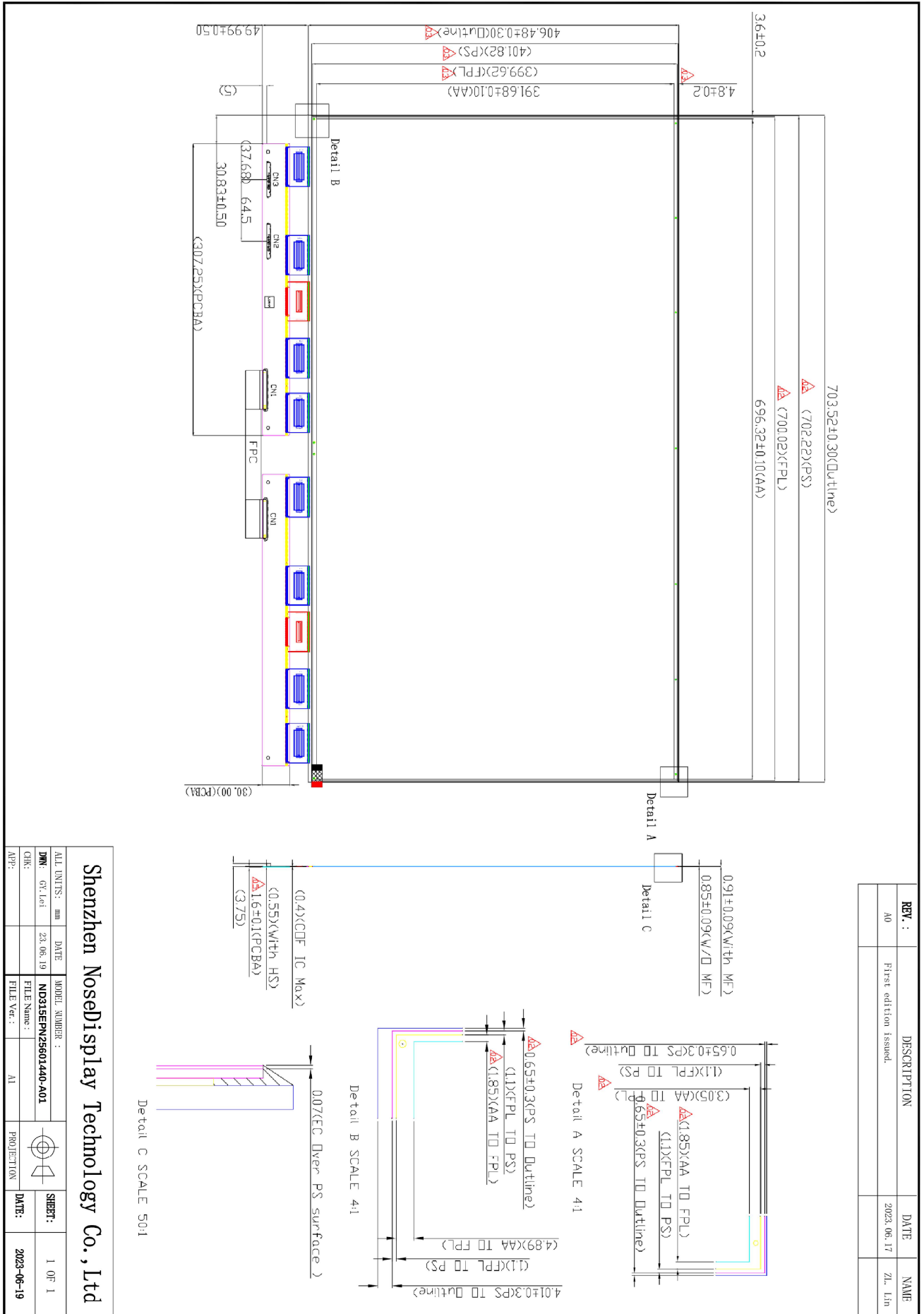
* General tolerance applies unless otherwise specified in the drawing.

2. Sample Reference Image



Sample image for reference. Displayed content and apparent colors depend on the image, waveform, lighting and viewing conditions.

3. Module Drawing



4. Interface and Electrical Summary

Interface: SPI with Single / Dual / Quad data transfer support. QSPI applies to R10h (DTM) data bytes; it is not a four-lane mode for all commands. See Sections 13 and 14 for configuration and reference wiring.

Connector type: P-TWO 187059-51221 compatible. The module has separate power and signal connections. Serial modes include 3-wire SPI, 4-wire SPI and standard 4-wire SPI, including quad data mode. RST_N is active low; BUSY_N = 0 indicates busy. TSCL and TSDA serve the external temperature sensor.

No.	Supply rail	Minimum	Typical	Maximum	Unit
1	VDD / AVDD	2.7	3.3	3.6	V
2	VCC	1.3	1.35	1.4	V
3	VGH	26	27	28	V
4	VGL	-21	-20	-19	V
5	VPOS1	14	15	16	V
6	VNEG1	-16	-15	-14	V

Selected normal operating rails only. The module also requires additional analog and common-voltage supplies. Apply the complete pin assignment, power sequence and assigned VCOM from the full technical specification; VDD alone is not a complete module power supply.

No.	Panel power	Reference value	Unit
1	Typical update power	1170.79	mW
2	Maximum update power	5541.75	mW
3	Standby power	165	mW

Power figures use the source specification's 50 Hz drive waveform and stated test patterns. Standby power depends on the controller and enabled power rails; these values do not describe the input power of a finished wireless system.

Reference: ED2208-QBA (ND320ENM-A01) Technical Specification, Version 1.0; sections 3–6, 8 and 9. This specification summarizes selection and integration parameters. Refer to the full specification for complete electrical limits, timing and reliability conditions.

4.1 Detailed Current Consumption

Operating current is the oscilloscope mean value. Test voltages and current values below are reproduced from the source DC characteristics. All current values are in mA; no minimum current is specified.

Current	Test voltage (V)	Minimum	Typical	Maximum	Inrush reference
IVDD	3.3	—	5.29	5.928	170
IAVDD	3.3	—	67.56	59.52*	230
IVCC	1.35	—	35.16	44.5	190
IVNCP_3P5	-3.5	—	2.95	5.196	170
IVBB_3P5	-3.5	—	4.82	5.376	210
IVGL	-20	—	7.776	44	1580
IVGH	27	—	7.188	6.82*	80
INEG1	-15	—	8.64	82.8	1400
INEG2	-8.5	—	5.76	12.96	200
INEG3	-8.6	—	4.7	16.7	220
IPOS1	15	—	4.09	78.72	1580
IPOS2	8.25	—	2.0	23.28	260
IPOS3	8.7	—	2.83	29.3	200
IVDDP	19	—	2.7	27	390
IVDDN	-19	—	6.46	27.48	330
TFT_ICOM	-1.09	—	4.41	1.716*	550
FPL_ICOM	-1.09	—	4.93	3.768*	1150

* Source inconsistency: IAVDD, IVGH, TFT_ICOM and FPL_ICOM have Typical values greater than their stated Maximum values. These entries have not been swapped or corrected. Confirm them with the module supplier before using them as power-supply design limits.

Inrush values are reference values only and depend on the controller drive capability. They are not additional steady-state currents. Currents on different voltage rails must not be summed to estimate the input current of a controller board.

4.2 Power Measurement Conditions

Typical power: 1170.79 mW at a 50 Hz waveform, transitioning from continuous white to basic color bars. Maximum power: 5541.75 mW using the source stress transition, equivalent to each pixel emerging from continuous white. The controller and waveform must match the supplier reference conditions.

Standby power: 165 mW, reported in the source Maximum column and dependent on the controller / EVK input power. VDD, VCC, VDDN, VDDP and VNCP remain on; the other supplies are off. This is not a guaranteed bare-module sleep current.

5. Handling and Integration

Handle the glass panel carefully. Avoid impact, twisting, uneven mounting pressure and force on the display surface. Provide a protective cover and a mounting structure that keeps the module within its specified temperature range.

Keep the module away from corrosive gases and do not disassemble it. Follow the full specification's surface-specific cleaning instructions; unsuitable solvents can damage the protective sheet.

6. Connector Pin Assignment

Connector: P-TWO 187059-51221 compatible. CON2 carries the serial interface and temperature-sensor signals. Pin ranges below group signals with the same function; retain the stated pin order when routing the interface.

Pin	CON2 signal	Function	I/O
1–4	R-CS0 / 1 / 2 / 3	Right-half serial chip selects	I/O
5	R-SCL	Right-half serial clock	I/O
6	R-D_CX	Command/data selection in 4-wire SPI	I/O
7	R-SI0	SDA / MOSI; quad data input	I/O
8	R-SI	MISO; quad data input	I/O
9–10	R-SI2 / R-SI3	Quad data inputs	I/O
11–14	NC	No connection	-
15–18	L-CS0 / 1 / 2 / 3	Left-half serial chip selects	I/O
19	L-SCL	Left-half serial clock	I/O
20	L-D_CX	Command/data selection in 4-wire SPI	I/O
21	L-SI0	SDA / MOSI; quad data input	I/O
22	L-SI1	MISO; quad data input	I/O
23–24	L-SI2 / L-SI3	Quad data inputs	I/O
25–27	NC	No connection	-
28	RST_N	Global reset; low = reset	I/O
29	BUSY_N	0 = busy; 1 = not busy	I/O
30	CL	Master clock output / slave clock input	I/O
31–42	NC	No connection	-
43–44	TSCL / TSDA	External temperature sensor I2C	-
45–51	NC	No connection	-

D_CX: low selects commands and high selects data in 4-wire SPI. Connect D_CX to GND in 3-wire or standard 4-wire mode. SPI data-line direction depends on the selected serial mode.

The complete PCB_L CON3 power connector assignment is provided below. P denotes a power or analog supply connection; G denotes ground.

6.1 CON3 Power Connector Pins 1 to 26

PCB_L connector: P-TWO 187059-51221 compatible. Pin numbers below follow the source connector assignment.

Pin	Signal	Type	Description
1	VSPHI	P	Positive source-driver supply.
2	VSPHI	P	Positive source-driver supply.
3	VSPHI	P	Positive source-driver supply.
4	VSPLI	P	Positive source-driver supply.
5	VSPLI	P	Positive source-driver supply.
6	VSPLI	P	Positive source-driver supply.
7	VSPL2I	P	Positive source-driver supply.
8	VSPL2I	P	Positive source-driver supply.
9	VSPL2I	P	Positive source-driver supply.
10	VSNHI	P	Negative source-driver supply.
11	VSNHI	P	Negative source-driver supply.
12	VSNHI	P	Negative source-driver supply.
13	VSNLI	P	Negative source-driver supply.
14	VSNLI	P	Negative source-driver supply.
15	VSNLI	P	Negative source-driver supply.
16	VSNL2I	P	Negative source-driver supply.
17	VSNL2I	P	Negative source-driver supply.
18	VSNL2I	P	Negative source-driver supply.
19	VPP	P	Source-driver OTP supply.
20	VPP	P	Source-driver OTP supply.
21	GND	G	Ground.
22	GND	G	Ground.
23	VGH	P	Positive gate-driver supply.
24	VGH	P	Positive gate-driver supply.
25	AVDD	P	DC/DC power input voltage.
26	AVDD	P	DC/DC power input voltage.

6.1 CON3 Power Connector Pins 27 to 51

PCB_L connector: P-TWO 187059-51221 compatible. Pin numbers below follow the source connector assignment.

Pin	Signal	Type	Description
27	AVDD	P	DC/DC power input voltage.
28	VDD	P	Analog / digital supply for source-driver IC.
29	VDD	P	Analog / digital supply for source-driver IC.
30	VCC	P	Common voltage for source-driver IC oscillator.
31	VCC	P	Common voltage for source-driver IC oscillator.
32	VDDN	P	Negative analog supply.
33	VDDN	P	Negative analog supply.
34	VDDN	P	Negative analog supply.
35	VGL	P	Negative gate-driver supply.
36	VGL	P	Negative gate-driver supply.
37	VDDP	P	Positive analog supply.
38	VDDP	P	Positive analog supply.
39	VDDP	P	Positive analog supply.
40	Boder	P	Border voltage-check output.
41	Boder	P	Border voltage-check output.
42	VCOMBD	P	Border buffer output; 0.47 μ F stabilization per application circuit.
43	VCOMBD	P	Border buffer output; 0.47 μ F stabilization per application circuit.
44	VNCP-3P5V	P	Negative analog supply for TFT VCOM.
45	VNCP-3P5V	P	Negative analog supply for TFT VCOM.
46	VBB-3P5V	P	Negative analog supply for TFT VCOM.
47	VBB-3P5V	P	Negative analog supply for TFT VCOM.
48	TFT-VCOM	P	Common voltage.
49	TFT-VCOM	P	Common voltage.
50	FPL-VCOM	P	Common voltage.
51	FPL-VCOM	P	Common voltage.

The source signal name “Boder” is retained for traceability and means Border. Pins 42 and 43 share the VCOMBD signal; apply the 0.47 μ F stabilization requirement according to the reference application circuit. Verify connector contact orientation against the mechanical drawing before PCB routing.

7. Optical Characteristics

No.	Parameter	Minimum	Typical	Unit
1	White reflectance	30	34	%
2	Contrast ratio	15	22	-
3	Image update time	-	15	s

8. Optical Color Performance

Typical CIELAB color coordinates at 25 °C are listed below. Measurements use 45° illumination with a detector perpendicular to the display. The source specifies an Eye-One Pro3 Plus spectrophotometer.

State	Color	L* typical	a* typical	b* typical	ΔE2000 max
WS	White	66.5	-4	0	6
DS	Dark	12	7	-11	6
RS	Red	26.5	41	30	6
YS	Yellow	62	-11	65	6
BS	Blue	34	3.5	-37	6
GS	Green	35	-22	15	8

Color difference uses CIEDE2000 (ΔE2000). The typical coordinates are the reference points. Contrast ratio is the ratio of full-white reflectance to dark-state reflectance. Typical full-image update time is 15 s at 25 °C with the specified controller and waveform.

9. Absolute Maximum Ratings

No.	Parameter	Minimum	Maximum	Unit
1	VDD	-0.3	+3.6	V
2	VCC	-0.3	+1.42	V
3	VDDP	-0.5	+21	V
4	VDDN	-21	+0.5	V
5	VPOS	-0.3	+17	V
6	VNEG	-17	+0.3	V
7	VPOS minus VNEG	-0.3	34	V
8	VGH	-0.3	+30	V
9	VGL	-25	+0.3	V
10	VGH minus VGL	0.3	55	V

Selected absolute maximum ratings are stress limits, not recommended operating conditions. Exceeding them can permanently damage the panel. Additional rails and limits must follow the complete source specification. Use the normal operating ranges in Section 4 for the listed rails.

10. Power Sequencing

The supply rails must follow the required sequence. The steps below preserve the rail order in the source specification; observe its timing diagram when implementing the controller.

Step	Power on	Power off	-
1	VDD / AVDD / VCC	VCOM	-
2	VDDN	VGH and positive/negative source rails	-
3	VDDP	VGL	-
4	VNCP_3P5	VNCP_3P5	-
5	VGL	VDDP	-
6	VSPHI / VSPLI / VSPL2I	VDDN	-
7	VSNIHI / VSNI / VSNI2I	VDD / AVDD / VCC	-
8	VGH	-	-
9	VCOM	-	-

The source timing intervals t_a – t_g for power on and t_h – t_n for power off each have a 100 μ s minimum. These intervals refer to the waveform diagram; they must not be treated as permission to ignore rail-discharge requirements.

10.1 Rail and Restart Requirements

1. VDDP must remain higher than the positive source-driver rails VSPHI, VSPLI and VSPL2I at all times.
2. VDDN must remain lower than the negative source-driver rails and VBB_3P5V / VNCP_3P5V at all times.
3. Discharge VNCP_3P5 and VBB_3P5 to 0 V before turning off VDDP and VDDN. Discharge VDDP and VDDN to 0 V before removing VDD / AVDD.
4. Before a fast restart, VDD / AVDD must fall below 0.2 V and VCC below 10% of its operating voltage. Complete VDDN power-off before beginning another power-on sequence.
5. During the specified 16K OTP load, BUSY_N stays low for t_1 ; the source gives a minimum t_1 of 30 ms. Check BUSY_N before sending the next operation.

10.2 Controller and Waveform

Use the panel-specific controller and waveform supplied for ND320ENM-A01. Set VCOM within ± 0.2 V of its assigned value. Additional source rails and common voltages are adjusted values, not universal fixed supplies. The internal maximum 50 Hz drive refresh rate is separate from the 15 s typical optical image update time.

10.3 Reference Power Sequence Diagram

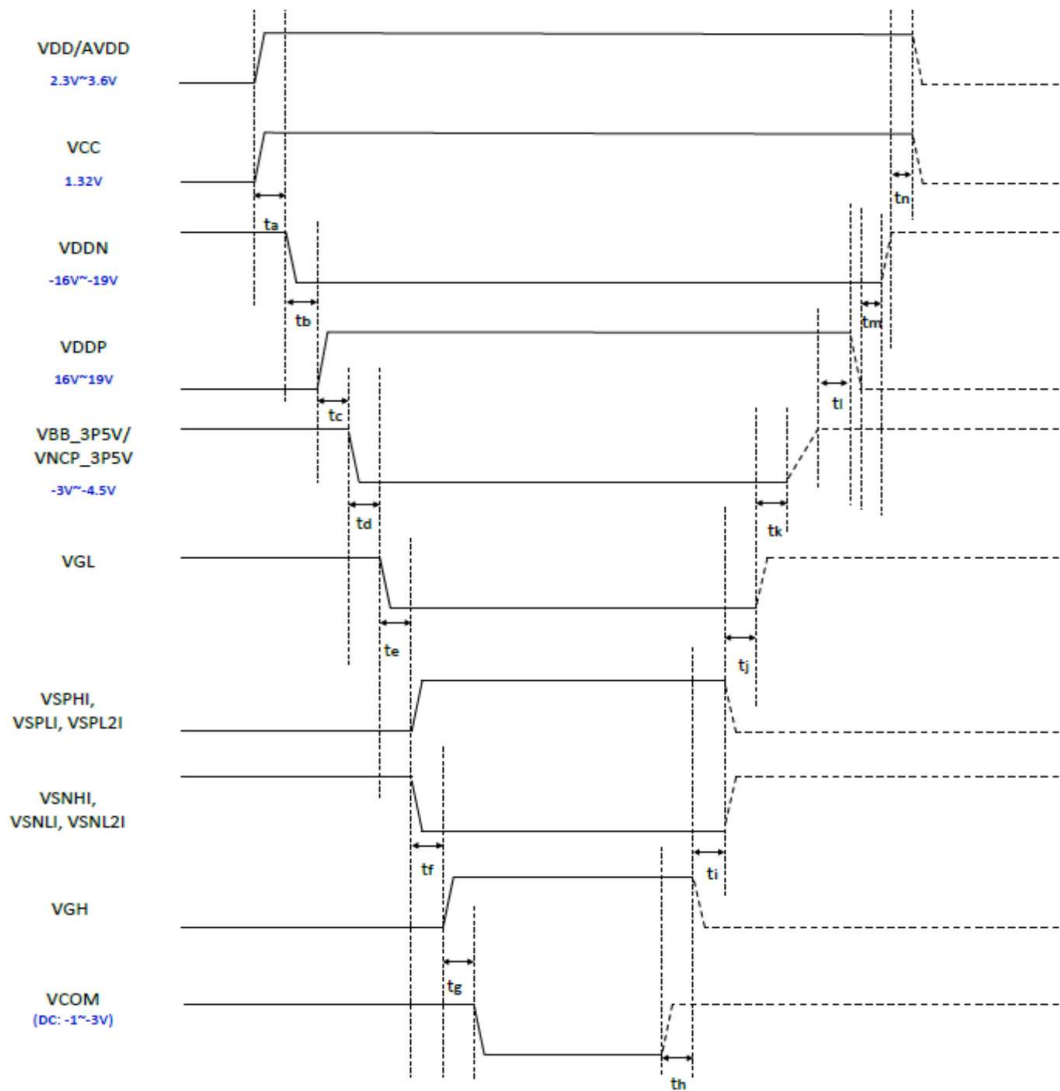


Figure 10.1 Power rail sequence. Timing intervals t_a through t_g (power-on) and t_h through t_n (power-off) each have a minimum of 100 μ s; no maximum is specified. The figure illustrates sequence relationships, not voltage selection. Use confirmed operating rail settings and the absolute limits in Section 9.

10.4 Discharge and Fast Restart Timing

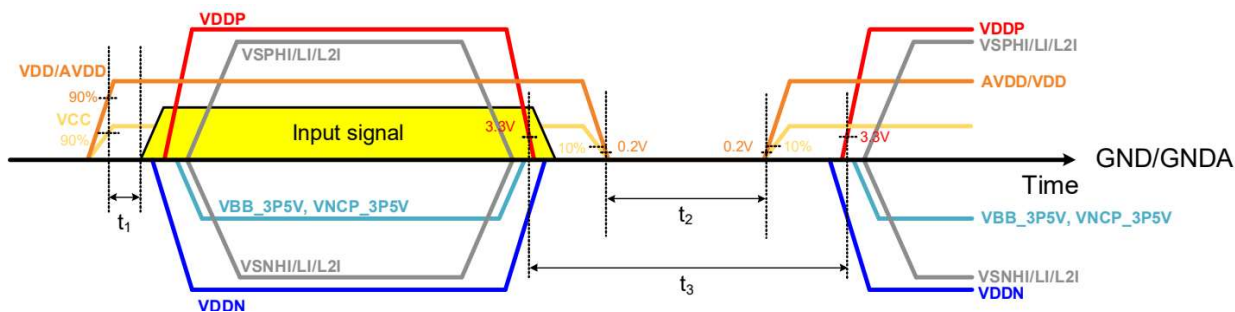


Figure 10.2 Supply discharge and restart reference. Complete discharge conditions as well as the timing minima before restarting.

Timing	Minimum	Typical	Maximum	Unit	Requirement
t1	30	—	—	ms	BUSY_N remains low during OTP loading at 16K.
t2	0	—	—	ms	Fast restart: VDD / AVDD below 0.2 V and VCC below 10% of operating voltage.
t3	0	—	—	ms	Fast restart: VDDP below 3.3 V.

A 0 ms minimum for t2 or t3 does not waive the associated voltage-discharge condition. VDDP must stay above the positive source rails; VDDN must stay below the negative source rails, VBB and VNCP. Discharge VNCP / VBB to 0 V before switching off VDDP / VDDN, and discharge VDDP / VDDN to 0 V before turning off VDD / AVDD.

11. Reliability Test Conditions

The following conditions summarize the source specification's module and shipping-package tests. They are test conditions rather than wider operating limits or a service-life guarantee.

No.	Test item	Condition	Time
1	High-temperature operation	+50 °C, 30% RH; 150 s update interval	240 h
2	Low-temperature operation	0 °C; 150 s update interval	240 h
3	High-temperature storage	+60 °C, 35% RH; white image	240 h
4	Low-temperature storage	-25 °C; white image	240 h
5	Humid operation	+40 °C, 90% RH; 150 s update interval	240 h
6	Humid storage	+60 °C, 80% RH; white image	240 h
7	Temperature cycling	-25 °C / +60 °C; 30 min at each; white image	50 cycles
8	Electrostatic effect	Non-operating; machine model ± 250 V, 0 Ω , 200 pF	-
9	Packaged vibration	1.5 Grms; 10–200 Hz; X, Y and Z	30 min/axis
10	Packaged drop	33 cm; 1 corner, 3 edges and 6 faces	-

Remove the protective film before temperature testing. Operation tests use a 150 s image-update interval. The functional acceptance criterion is no display failure such as line defects or missing images under standard conditions. Cosmetic inspection is evaluated before reliability stress. Application-level EMC must be measured in the final system.

12. Storage and Assembly Notes

Maintain operating temperature between 0 and +50 °C and storage temperature between -25 and +60 °C. Use a mechanically supported enclosure, avoid panel bending, and protect the display face from hard objects. Keep liquids, corrosive gases and incompatible case materials away from the module.

Do not apply a general-purpose solvent across the entire module. The source restricts IPA to the active area and back of the glass, while also giving protective-sheet-specific solvent exclusions. Confirm the surface material and approved cleaning procedure before cleaning. Do not disassemble the module.

Source reference: ND320ENM-A01 Technical Specification, Version 1.0. CON3 pin definitions, reference power and serial timing, and current consumption are reproduced in Sections 6, 10, 13 and 4 respectively. Confirm unresolved source values with the supplier before hardware design.

13. QSPI Support and Configuration

ND320ENM-A01 supports Quad Data SPI (QSPI). The source explicitly defines Single, Dual and Quad data transfer in register E6h (SPIM). This is a selectable capability; the installed controller wiring and initialization determine the actual operating mode.

Mode	SPIM bits [1:0]	Valid data lines	Value
Single	00	D0	00h
Dual	01	D0 and D1	01h
Quad	10	D0, D1, D2 and D3	02h
Single	11	D0	03h

The E6h setting affects only the data bytes associated with R10h (DTM). Do not send every command, register parameter or read transaction as four-lane data. The controller must support the required command and data phases.

13.1 Hardware Mode Selection

No.	Bus mode	BS0	BS1	D_CX
1	3-wire SPI	L	L	GND
2	4-wire SPI with D/C	H	L	D/C
3	Standard 4-wire SPI	H	H	GND

H means VDD and L means GND. The reference connection uses standard SPI with four data lines available for the quad data phase. The BS0 / BS1 selection points are described in the source, but are not assigned CON2 connector pins; confirm the module or controller-board straps before use.

13.2 Configuration Outline

1. Confirm standard SPI hardware selection and connect all four data lines for each required panel half. Apply the approved power sequence and controller initialization with the panel-specific waveform.
2. Send E6h (SPIM) with parameter 02h through the required command/parameter transaction. Configure each addressed source-driver channel as required by the panel controller.
3. For R10h (DTM), use the prescribed command phase, then transfer the affected image-data bytes on D0–D3. Preserve the required chip-select timing and monitor BUSY_N.

Ordinary “4-wire SPI” describes clock, serial data, chip select and D/C in this source. It must not be used as a synonym for QSPI. These steps describe mode selection, not a complete display initialization or waveform implementation.

13.3 Standard 4 Wire SPI Reference Timing

These diagrams apply to standard 4-wire SPI with separate MOSI and MISO and D_CX tied low. They show single-lane command, parameter, write and read transactions. Quad mode remains limited to R10h DTM data bytes as described in Section 13.2.

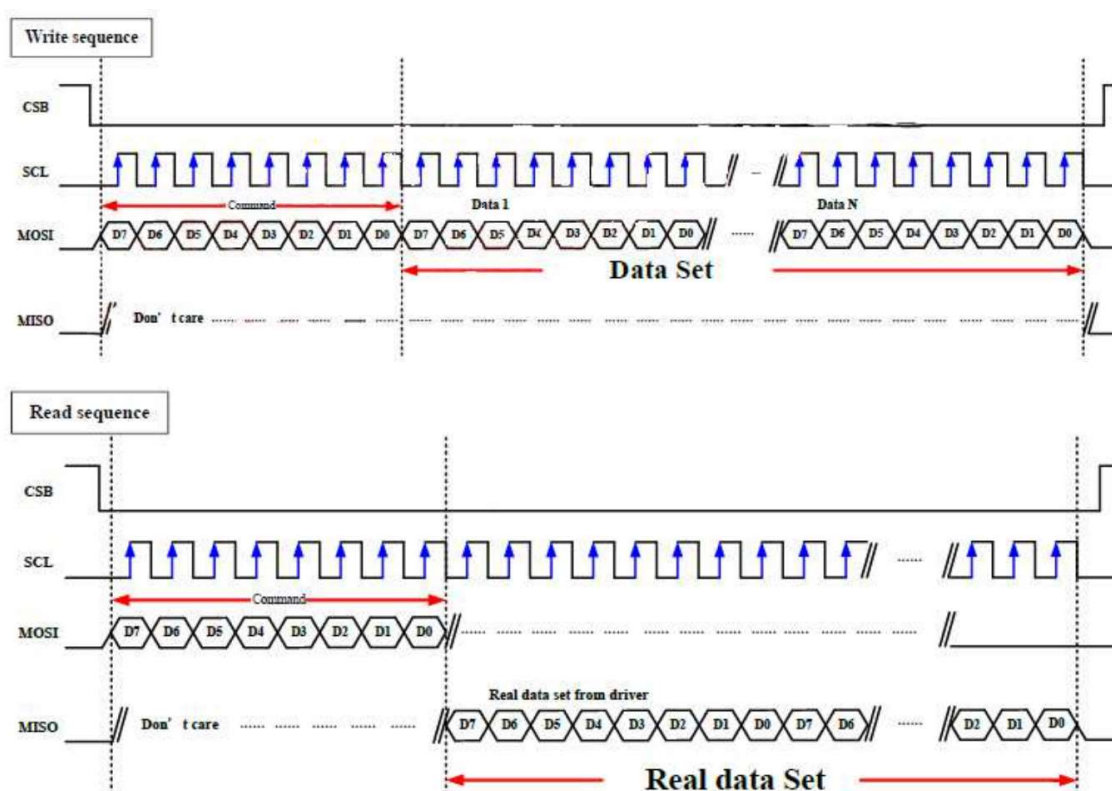
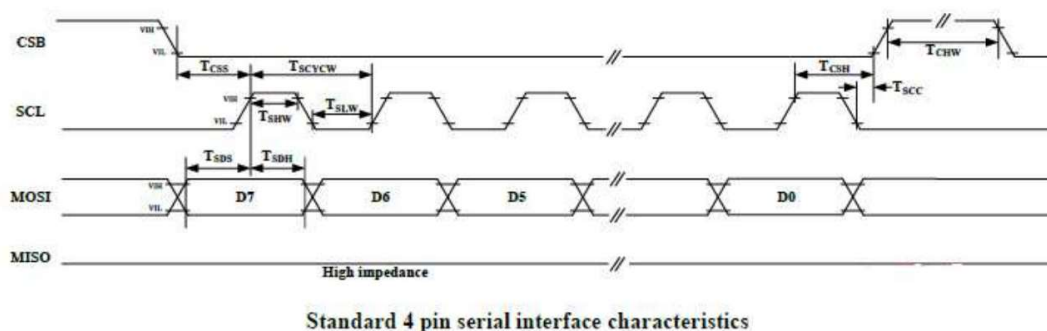


Figure : Standard 4 pin serial interface protocol

Figure 13.1 Standard 4-wire SPI timing and write / read sequences. This source figure is not a four-lane QSPI timing diagram.

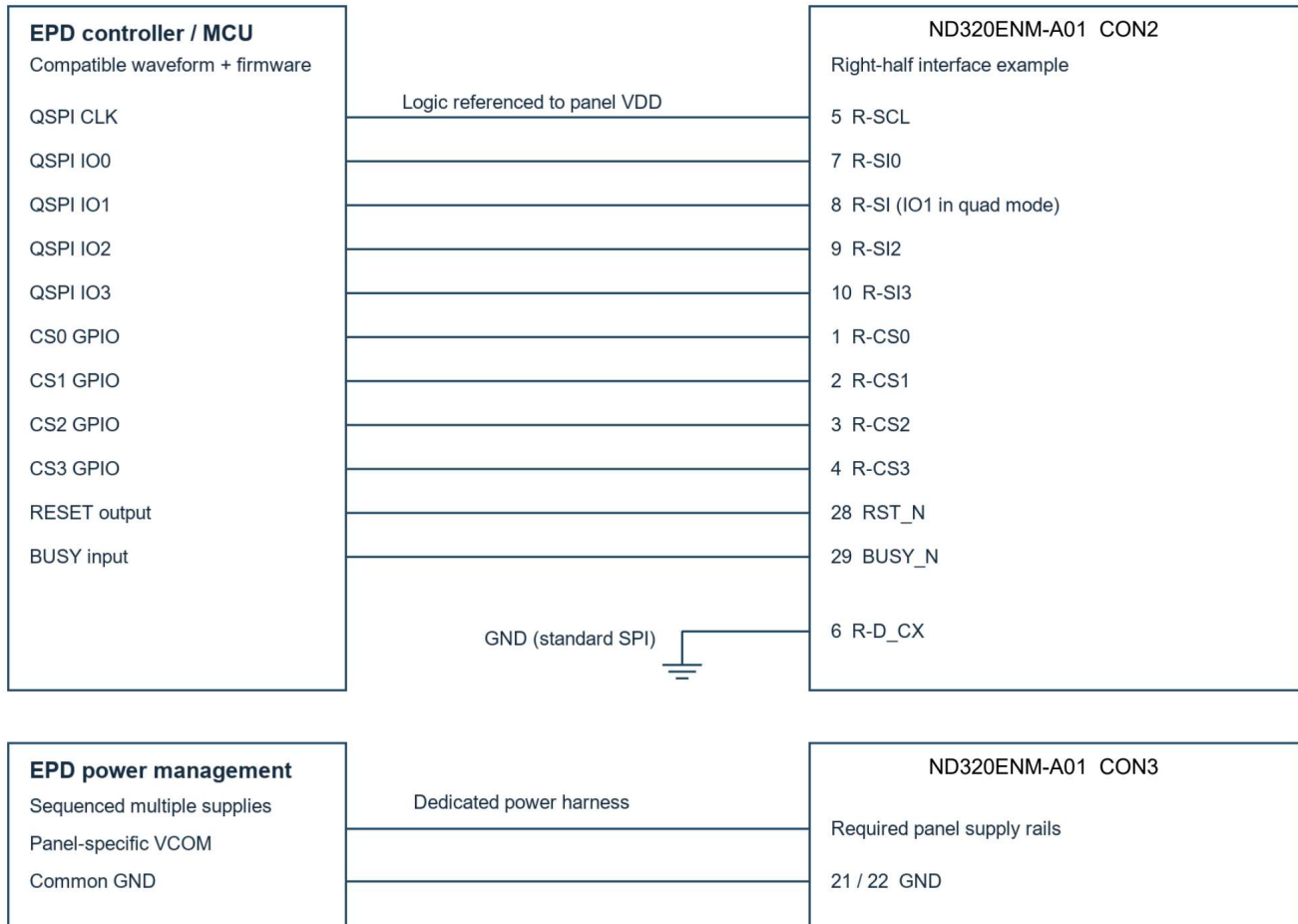
13.4 Standard 4 Wire SPI Timing Limits

Symbol	Minimum	Typical	Maximum	Unit	Description
Tcss	60	—	—	ns	Chip-select setup
Tcsh	65	—	—	ns	Chip-select hold
Tscc	20	—	—	ns	Chip-select setup
Tchwh	40	—	—	ns	Chip-select setup
Tscycw	100	—	—	ns	Serial clock period for write
Tshw	25	—	—	ns	Clock high width for write
Tslw	25	—	—	ns	Clock low width for write
Tscysr	200	—	—	ns	Serial clock period for read
Tshr	60	—	—	ns	Clock high width for read
Tslr	60	—	—	ns	Clock low width for read
TSCYC_CMD_PAR	150	—	—	ns	Clock period between command and first parameter
Tsds	30	—	—	ns	Data setup
Tsdh	30	—	—	ns	Data hold
TACC	—	—	140	ns	MISO access time
TBYS	—	—	150	ns	BUSY_N setup time

Values and column assignments follow the source standard 4-wire timing table. TACC and TBYS are stated in the Maximum column. No dedicated four-lane QSPI AC timing table is provided in the source; confirm the controller waveform and validated QSPI clock setting before implementation.

14. Simple QSPI Connection Reference

The diagram shows right-half signal wiring to CON2 and the separate power harness to CON3. Use a compatible EPD controller, or an MCU implementation with the required panel firmware and waveform. This is a connection reference, not a complete power-supply schematic.



Reference wiring only. Left-half signals, CL and temperature sensor: see accompanying notes.

Left-half equivalent: CLK → pin 19; IO0/1/2/3 → pins 21/22/23/24; CS0/1/2/3 → pins 15/16/17/18; D_CX pin 20 → GND in standard SPI. Route the two halves according to the controller architecture; do not short their signals together without validating bus sharing and chip-select behavior.

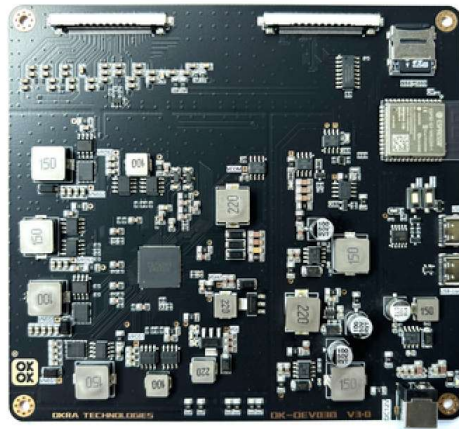
RST_N pin 28 and BUSY_N pin 29 are shared control/status connections. CL pin 30 is a master/slave clock connection and must follow the approved controller configuration; it is not the SPI clock. TSCL / TSDA pins 43 / 44 connect to the external temperature-sensor circuit. These connections are omitted from the simplified drawing, not designated unused.

Use logic levels referenced to VDD (3.3 V typical). Connect controller and panel power grounds. A single 3.3 V supply is insufficient: CON3 needs the specified positive, negative and common-voltage rails with sequencing. Keep separate chip selects independently controlled; leave NC pins unconnected.

Source basis: Version 1.0, pages 6–8, 14, 23–26 and 32. The diagram is a simplified engineering reference derived from the pin table and block diagram; confirm the selected controller hardware before PCB release.

15. Evaluation Board Reference

For customer reference only. The OK-DEV03A evaluation board is a separate accessory and is outside the display module specification. Its features and ratings do not define or extend the module ratings.



No.	Board parameter	Reference information	Unit
1	Board model	OK-DEV03A	-
2	Platform	ESP32-S3	-
3	Function	Driver board / main board	-
4	Intended display	31.5 inch Spectra 6 e-paper display	-
5	Board width	140.0	mm
6	Board height	100.0	mm
7	Interface	USB Type-C	-
8	Power input	12	V DC
9	Wireless communication	Wi-Fi and Bluetooth	-
10	Listed grayscale capability	Up to 16 levels (board reference)	-
11	Listed operating temperature	-25 to +60 (board only)	°C
12	Other listed features	LED indicator; user button; reset; flash; current detection	-

Reference functions: display driving, testing and evaluation; image demonstration; supplied TF card with one-click slideshow; secondary development support.

The module operating range remains 0 to +50 °C. The board's listed grayscale capability is not a grayscale specification for this six-color module. Confirm the board configuration and power connection before use; the listed USB Type-C interface does not by itself establish how the 12 V input is supplied.

15.1 Evaluation Kit Application

Application illustration for customer reference only. The evaluation kit and its software features are outside the display module specification.



Application illustration: 31.5-inch display connected to the evaluation board.

ND320ENM-A01 is a 31.5-inch full-color E Ink display with a resolution of 2560×1440 pixels. Compared with ACeP technology, it offers improved color performance and faster image updates. It is expected to become a mainstream option for digital photo frames, signage boards and related products.

The evaluation kit is equipped with a motherboard based on the ESP32-WROOM-S3-1-N16R8 Bluetooth/Wi-Fi module, making it convenient for developers to debug EPD driver code. Images can be transferred directly from a TF card or an Android application to the display, allowing quick and intuitive demonstrations of the display performance.

The comparison, market outlook and software capabilities above describe the supplied evaluation-kit application information. They do not add guaranteed performance limits to the display module specification.

15.2 Evaluation System Application Block Diagram

CUSTOMER REFERENCE ONLY. The following application block diagram illustrates an external EPD controller with Flash and power management connected to the display through CON2 and CON3. The controller, Flash and power-management board are evaluation-system components and are outside the module specification and standard module scope.

11. Block Diagram

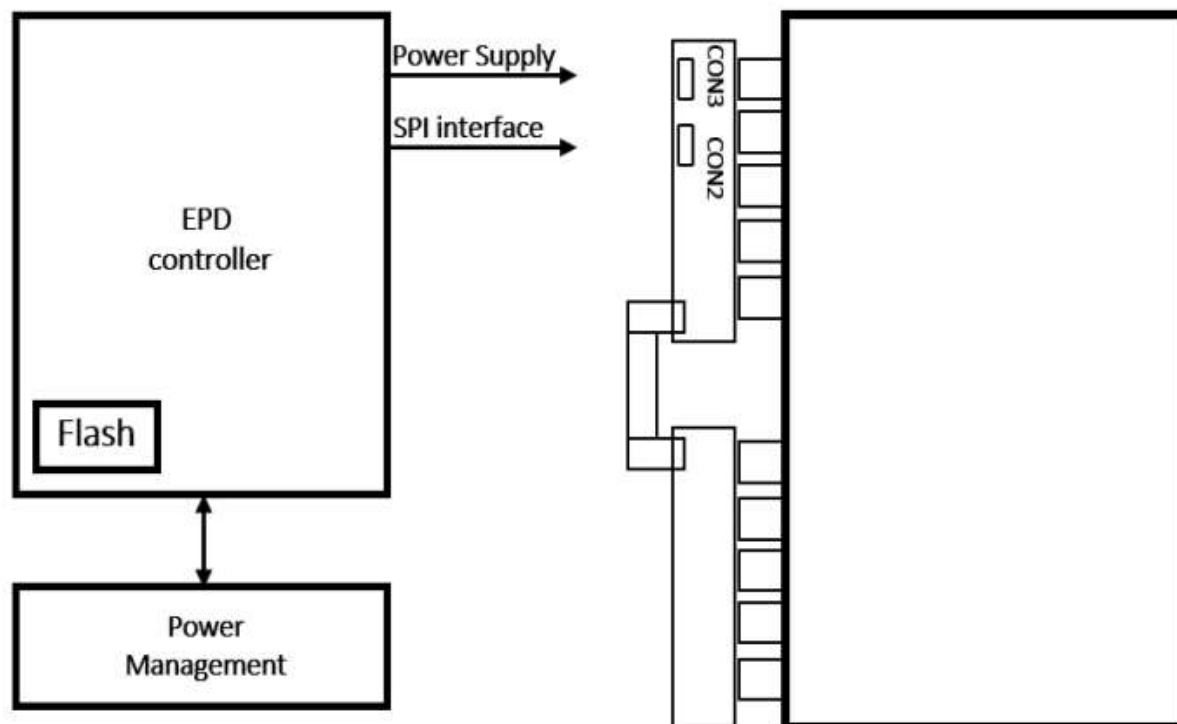


Figure 15.2 Evaluation system application diagram supplied for customer reference. The “11. Block Diagram” heading belongs to the supplied screenshot; this figure is part of Section 15 of this document.

CON3 carries the module power rails; CON2 carries the serial interface and related signals. The blocks show functional relationships only, not a complete circuit, connector contact orientation or a guarantee that evaluation-board accessories are included with the module.